

FORM PTO-1449
(Rev. 7-80)

U.S. Department of Commerce
Patent and Trademark Office

Attorney Docket No.:
TESSERA 3.0-030 CIP V DIV
CONT

Serial No.:
Unassigned

LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)

Applicant:
DiStefano, et al.

Filing Date:
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Group:

Sheet 1 of 5

15421 U.S. PRO
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U.S. PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
MC	AA	5,528,083	6/18/96	Malladi et al			
	AB	4,142,288	3/6/79	Flammer et al			
	AC	4,326,663	4/27/82	Oettel			
	AD	4,520,562	6/4/85	Sade et al			
	AE	4,661,192	4/28/87	McShaen			
	AF	4,667,219	5/19/87	Lee et al			
	AG	4,751,199	6/14/88	Phy			
	AH	4,893,172	1/9/90	Matsumoto et al			
	AI	4,955,523	9/11/90	Calomagnio et al			
	AJ	5,049,085	9/17/91	Reylek et al			
MC	AK	5,057,460	10/15/91	Rose			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES NO
MC	AL	2142568A		United Kingdom			
	AM	2151529A		United Kingdom			
	AN	0072673A2		Europe			
	AO	6191939		Japan			
MC	AP	3-108734 **		Japan			X

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

MC	AR	"Method of Testing Chips and Joining Chips to Substrates", Research Disclosure, February 1991, Number 322, Kenneth Mason Publication Ltd., England
		IBM Technical Disclosure Bulletin, Vol. 36, No. 07, July 1993
	AS	
	AT	
EXAMINER		DATE CONSIDERED 7/10/03

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mc	AA	4,067,04	1/10/78	Tracy			
	AB	3,811,186	5/21/74	Larned et al			
	AC	4,447,857	5/8/84	Marks et al			
	AD	4,954,877	9/4/90	Fox et al			
	AE	3,795,037	3/5/74	Lutmer			
	AF	4,949,158	3/14/90	Ueda			
	AG	4,954,877	9/4/90	Nakanishi et al			
	AH	3,373,481	3/19/68	Lins et al			
	AI	5,197,892	3/30/93	Yoshizawa et al			
	AJ	4,926,241	5/15/90	Carey			
mc	AK	4,793,814	12/27/88	Zifcak et al			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES NO
mc	AL	1-155633 **		Japan			X
mc	AM	WO 96/02068 **	01/96	WIPO			
	AN						
	AO						
	AP						

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*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
mc	AA	5,067,007	11/19/91	Kanji, et al			
	AB	5,166,099	11/24/92	Ueda et al			
	AC	5,254,811	11/19/93	Ludden, et al			
	AD	5,286,680	2/15/94	Cain			
	AE	5,346,861	9/13/94	Khandros, et al			
	AF	3,952,404	4/27/76	Matunami			
	AG	5,086,337	2/4/92	Noro et al			
	AH	5,192,716	3/9/93	Jacobs			
	AI	5,055,907	10/8/91	Jacobs			
	AJ	4,812,191	3/14/89	Ho et al			
mc	AK	4,721,995	1/26/88	Tanizawa			

FOREIGN PATENT DOCUMENTS

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							YES NO
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U.S. PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
MC	AA	5,152,695	10/6/92	Grabbe et al			
	AB	5,173,055	12/22/92	Grabbe			
	AC	5,047,830	9/10/91	Grabbe			
	AD	5,131,852	7/21/92	Grabbe et al			
	AE	5,230,931	7/27/93	Yamazaki et al			
	AF	4,629,957	12/16/86	Walteis et al			
	AG	4,785,137	11/15/88	Samuels			
	AH	5,210,939	5/18/93	Mallik et al			
MC	AI	3,825,353	07/23/74	Loro			
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

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							YES NO
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*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	AA	Re. 35,119	12/95	Blonder et al.			
	AB	4,937,653	06/90	Blonder et al.			
	AC	5,455,390	10/95	DiStefano et al.			
	AD	3,842,189	10/74	Southgate			
	AE	5,148,265	09/92	Khandros et al.			
	AF	5,148,266	09/92	Khandros et al.			
	AG	5,518,964	05/96	DiStefano et al.			
	AH	5,663,106	9/2/97	Karavakis, et al.			
	AI	5,776,796	7/7/98	DiStefano, et al.			
	AJ	5,929,517	7/27/99	DiStefano, et al.			
AK							

FOREIGN PATENT DOCUMENTS							
DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
					YES	NO	
AL	EP 0 352 020 A3	01/90	Europe				
AM	EP 0 433 997 A2	06/91	Europe				
AN	WO 94/03036	02/94	WIPO				
AO							
AP							

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	AR	Research Disclosure No. 322 (February 1991) "Method of Testing Chips and Joining Chips to Substrates," XP 000169195.
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